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BTEC & SCOTEC GUIDANCE FOR STUDENTS

Contents

BUSINESS AND TECHNICAL EDUCATION COUNCIL

Certificate Programme in Telecommuncations

Sets of model questions and answers for Business and Technician Education Council (BTEC) units are given below. The questions illustrate the types of questions that students may encounter, and are useful as practice material for the skills learned during the course.

Where additional text is given for educational purposes, it is shown within square brackets to distinguish it from information expected of students under examination conditions. Representative time limits are shown for each question, and care has been taken to give model answers that reflect these limits.

We would like to emphasise that the questions are not representative of questions set by any particular college.

BTEC: TELEPHONE SWITCHING SYSTEMS II

The following questions are based on the BTEC's standard unit U81/753. Students are advised to read the notes above

Q1 Choose the correct statement to complete the following sentence. Traffic intensity in erlangs is defined as the ..... of simultaneous calls in progress.

(a) highest number,
(b) lowest number,
(c) average number,
(d) aggregate number, or
(e) average proportion *(2 min)*

A1 (c) average number

Q2 State two factors which may contribute to the shape of a telephone exchange traffic graph over a period of 24 h and briefly explain the effect of each factor *(10 min)*

A2 (a) The type of customer served by the exchange; that is, business or residential. Business customers tend to generate mid-morning and mid-afternoon traffic peaks, while residential customers are mainly responsible for evening peaks where advantage is taken of cheap-rate tariffs.

(b) The location of the exchange. For example, an exchange serving an area of specific industry such as a fishing community may well have a traffic peak in the early hours of the morning because of traffic to and from fish markets.

Q3 The factor controlling the provision of exchange equipment and junction line plant is ..... (Choose the one correct answer from the following)

(a) the total number of calls handled in a 24 h period,
(b) the forecast busy-hour traffic at the design date,
(c) the grade of service provided, or
(d) the size of the building which is available. *(2 min)*

A3 (b) the forecast busy-hour traffic at the design date.

Q4 Define the term 'grade of service'. *(2 min)*

A4 The grade of service (GOS) of an item of telephone exchange equipment is the ratio of the traffic lost from that equipment to the traffic offered to it; that is,

$$\text{GOS} = \frac{\text{traffic lost}}{\text{traffic offered}}.$$

[*Tutorial note*: If it is assumed that all calls have the same duration, then

$$\text{GOS} = \frac{\text{calls lost}}{\text{calls offered}}.\ ]$$

Q5 Explain the difference between the terms 'concentration' and 'distribution' in telephone-exchange structure. *(10 min)*

A5 A typical telephone exchange serves several thousand customers and it would be highly uneconomical to provide each customer with individual routeing equipment because of its complexity and cost. Also, since only a limited number of the customers connected to an exchange will be making simultaneous calls, it is more economical to *concentrate* the traffic from all customers to a limited amount of routeing equipment. After a call has been routed through the exchange, it is necessary to *distribute* the calls to the desired line by expanding the limited number of routes to give access to all the exchange customers.

Q6 Give one example each of a concentrator switch and a distributor switch in

(a) a strowger exchange, and
(b) a TXK1 exchange. *(3 min)*

A6 (a) An example of a concentrator switch is a subscriber's uniselector; an example of a distributor switch is a final selector.

(b) A distributor switch B (DSB) is an example of both a concentrator switch and a distributor switch in a TXK1 exchange.

Q7 Explain briefly why a 4-digit local director telephone exchange can serve 10 000 lines, while a 4-digit non-director telephone exchange has a limit of about 6000 lines. *(5 min)*

A7 In a director telephone exchange, access to STD, outgoing local junctions and services is provided from first code selector levels. The numerical selectors can therefore provide access to local customers off all their levels, allowing the full numbering range of 0000–9999 to be used. In a non-director telephone exchange, because all access is provided from the first group selector levels, certain levels must be reserved for STD access (level 0), access to outgoing junctions (levels 8 and 9) and service calls (level 1). Thus only levels 2–7 are available for local subscriber access, allowing only the numbers 2000–7999 to be used.

Q8 *Give typical values for the grade of service at the points shown in Fig. 1.* *(4 min)*

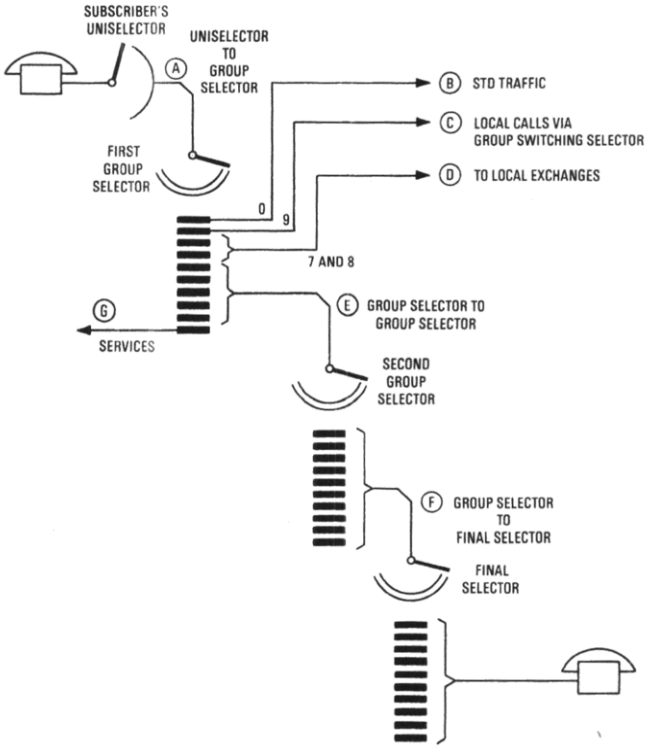


Fig. 1

A8 (A) 0·005
(B) 0·005
(C) 0·005
(D) 0·01
(E) 0·005
(F) 0·02
(G) 0·01

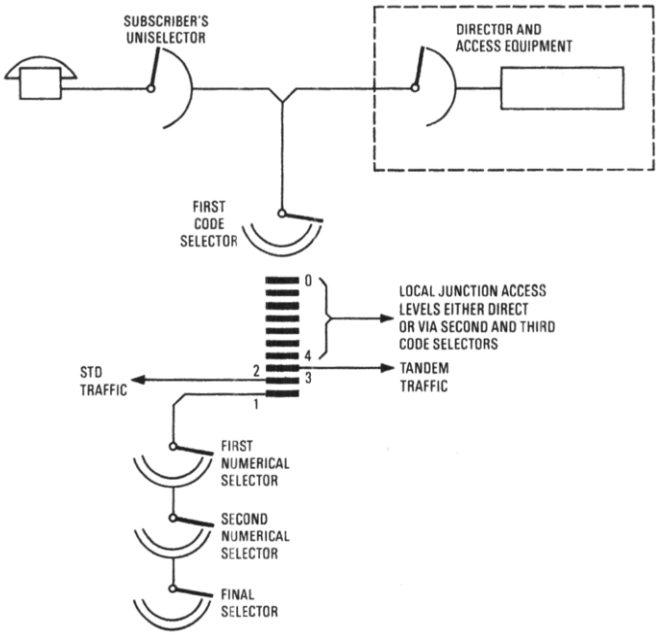
Q9 *On a call involving 2 translated routeing digits in a director area, the number of two-motion selectors held throughout the conversation period is*

(a) 2,
(b) 4,
(c) 5,
(d) 6, or
(e) 7. *(1 min)*

A9 (*d*) 6.

Q10 *Sketch a trunking diagram of a local director telephone exchange, showing subscribers' uniselectors, first code selectors, directors and access equipment. Indicate typical STD, tandem exchange and local junction access levels.* *(10 min)*

A10



[*Tutorial note*: In practice, the STD and tandem access levels could be any first code (or second code) selector levels, but early levels are usually chosen since both routes are likely to be high-traffic routes.]

Q11 *Fig. 2 shows the STD arrangements in a non-director group switching centre. Identify the blocks labelled A to E.* *(2 min)*

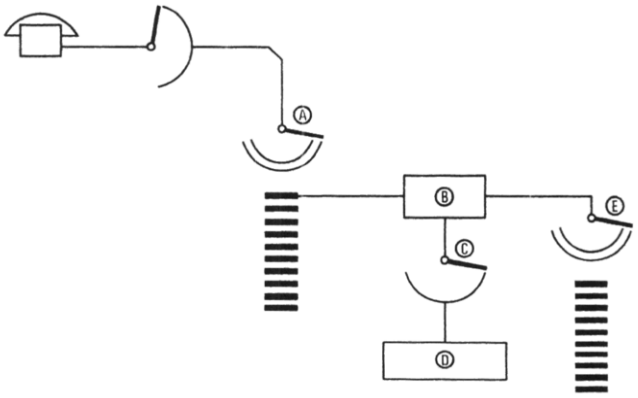


Fig. 2

A11 (A) First group selectors
(B) Register access relay-set
(C) Register hunter
(D) Register-translator
(E) Outgoing trunk first selector

Q12 *Match the following descriptions of items of equipment in a TXE2 telephone exchange with the given list of equipment.*

Descriptions

(a) Equipment needed for setting up each call in which the calling customer's dialled digits are stored.

(b) Equipment which identifies the calling customer and selects a free register.

(c) Call-path equipment which applies ringing current and ringing tone as well as metering the call throughout its duration.

(d) Circuits connecting different switching stages together.

(e) Equipment which is responsible for handling the whole call set-up operation.

(f) Equipment which converts calling and called customers' numbers from the form stored in the register to a directory form more suitable for marking the positions of the customers on the A-switches.

List
(*i*) *Links*
(*ii*) *Decoder*
(*iii*) *Register*
(*iv*) *Calling-number generator*
(*v*) *Supervisory relay-set*
(*vi*) *Call control*

(*4 min*)

A12

(*a*)	(*b*)	(*c*)	(*d*)	(*e*)	(*f*)
(*iii*)	(*iv*)	(*v*)	(*i*)	(*vi*)	(*ii*)

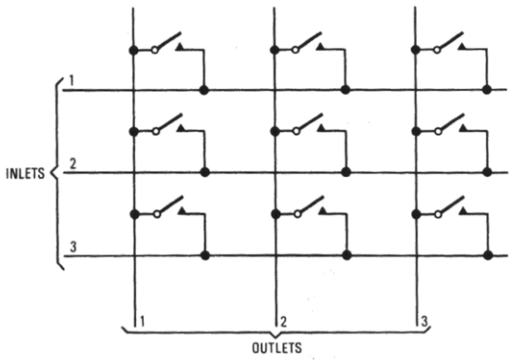
Q13 *In a TXE2 telephone exchange, the call control is involved with a call .....*

(*a*) *during selection of a register,*
(*b*) *during path selection,*
(*c*) *throughout the duration of a call,*
(*d*) *during receipt of dial pulses, or*
(*e*) *until the called customer answers.* (*2 min*)

A13 (*b*) during path selection.

Q14 *Draw a diagram of a 3 × 3 matrix switch showing how any inlet can be connected to any outlet. Name a suitable switching device which can be used at each crosspoint.* (*4 min*)

A14



The crosspoint contacts can be either relay-type contacts operated by an electromechanical crossbar switch or reed-relay insert contacts contained within an operating coil.

Q15 *State the three different categories of supervisory relay-set in a TXE2 telephone exchange.* (*1 min*)

A15 (*a*) outgoing
(*b*) incoming
(*c*) own-exchange

Q16 *The main reason for using several small interconnected matrix switches rather than one large single matrix is .....*

(*a*) *to keep the switch size small,*
(*b*) *to reduce the number of crosspoints used,*
(*c*) *to make call tracing easier, or*
(*d*) *to minimise exchange power consumption.* (*1 min*)

A16 (*b*) to reduce the number of crosspoints used.

Q17 *Fig. 3 shows a 15 × 15 matrix switch using three 6 × 4 A-switches and three 3 × 5 B-switches. Complete the diagram by inserting nine A–B links and three inter-aid links between the A-switches.* (*6 min*)

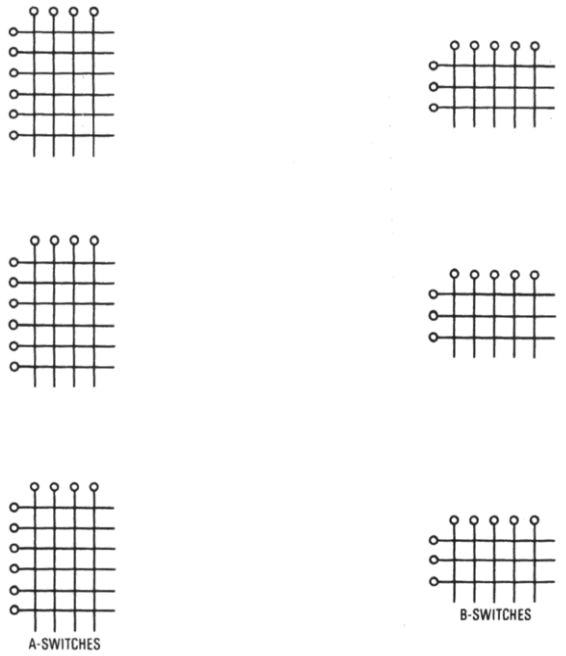
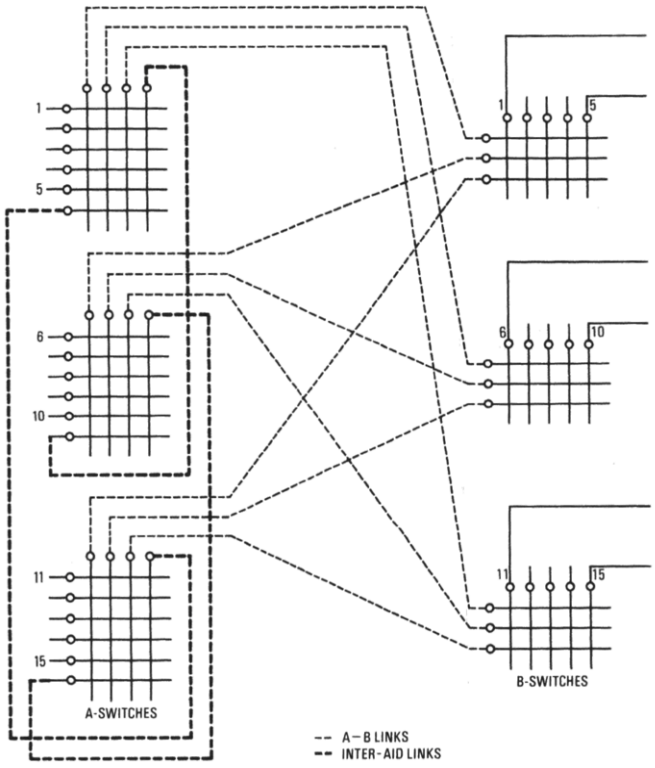


Fig. 3

A17

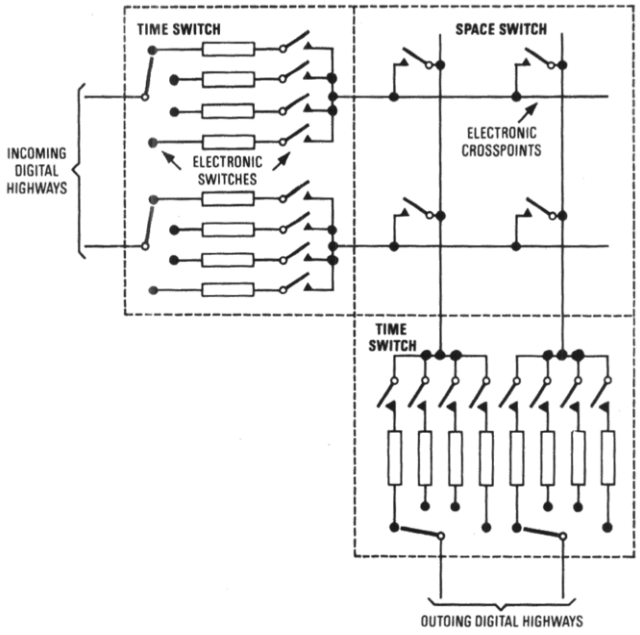


Q18 *What is the purpose of the inter-aid links in Q17?* (*1 min*)

A18 To reduce internal blocking.
[*Tutorial note*: Even if the 3 links from an A-switch to each B-switch are in use, there is still access to other B-switch inlets via the inter-aid link and the A–B links of the aiding A-switch.]

Q19 *Draw a simple switching network to show how two incoming 4-channel digital systems can be switched to two outgoing systems by using a time-space-time digital switch.* (*10 min*)

A19



Q20 Match the following descriptions in list A with the correct statements in list B.

List A

(*a*) *The signalling system over which dial pulses are sent from a telephone dial to a telephone exchange.*
(*b*) *A signalling system in which line current is always present, either in one direction or the other.*
(*c*) *A signalling system in which a number of different frequencies are used.*
(*d*) *A signalling system in which current flows in only one direction.*
(*e*) *A signalling system in which DC control signals are converted to AC, sent to the distant end and then reconverted to DC.*

List B

(*i*) *double-current signalling*
(*ii*) *single-current signalling*
(*iii*) *loop-disconnect circuit*
(*iv*) *multi-frequency signalling*
(*v*) *AC signalling system*

(4 min)

A20

(*a*)	(*b*)	(*c*)	(*d*)	(*e*)
(*iii*)	(*i*)	(*iv*)	(*ii*)	(*v*)

Q21 State a typical application of each of the following signalling methods.

(*a*) *loop-disconnect signalling,*
(*b*) *double-current signalling,*
(*c*) *single-frequency signalling, and*
(*d*) *multi-frequency signalling.* *(4 min)*

A21 (*a*) Local-line signalling between a customer and a telephone exchange.
(*b*) Five-unit code signals in a Telex system.
(*c*) Signalling over amplified circuits between group switching centres.
(*d*) High-speed signalling (SSMF2) between transit switching centres.

Q22 Several components are missing from the diagram of a telephone circuit shown in Fig. 4. Complete the diagram by inserting the correct circuit symbols for the missing components. *(4 min)*

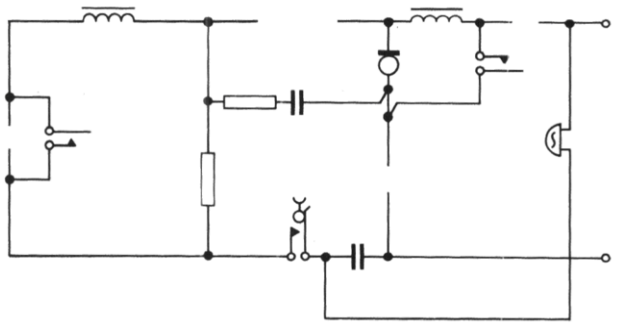
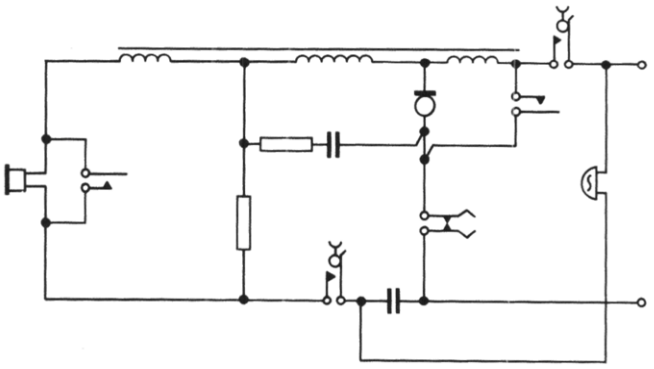


Fig. 4

A22



Q23 The shunting effect of the regulator in a telephone instrument is

(*a*) *great on short lines,*
(*b*) *negligible on short lines,*
(*c*) *great on long lines, or*
(*d*) *greater on long lines than on short lines.* *(2 min)*

A23 (*a*) great on short lines

Q24 What type of signalling is produced by the operation of the dial at a Telex station? *(2 min)*

A24 Double current; ±80 V signal potentials.

BTEC: MICRO-ELECTRONIC SYSTEMS II

The following questions are based on the BTEC' standard unit U79/603. Students are advised to read the notes on p. 33

[*Tutorial note:* Some of the questions given below require a knowledge of the mnemonics and machine code of a specific microprocessor. It would clearly be impossible to duplicate all such questions and answers for a range of microprocessors. Therefore, the Zilog Z80 has been chosen as a representative microprocessor because of its widespread use and machine-code compatability with the Intel 8080 and 8085. Students who have studied the Rockwell 6502 or Motorola 6800 should not find too much difficulty in adapting the questions for those microprocessors.]

A shortened instruction set for the Z80 is given below.

Mnemonic	Hexadecimal Code	Comment
LD A, *n*	3E *n*	Load the accumulator (register A) with data *n*.
LD A, B	78	Load the accumulator with the contents of register B.
LD B, *n*	06 *n*	Load register B with data *n*.
LD B, A	47	Load register B from the accumulator.
LD C, A	4F	Load register C from the accumulator.
LD HL, *nn*	21 *n n*	Load register pair HL with the number *nn*.
LD A, (HL)	7E	Load the accumulator from address (HL)
LD (HL), A	77	Load address (HL) from the accumulator.
ADD A, (HL)	86	Add the contents of address (HL) to the accumulator.
ADD A, B	80	Add the contents of register B to the accumulator.
AND B	A0	Logical AND the contents of register B with the contents of the accumulator.
SUB *n*	D6 *n*	Subtract number *n* from the accumulator.
INC HL	23	Increment register pair HL by 1.
INC A	3C	Increment the accumulator by 1.
INC B	04	Increment register B by 1.
DEC HL	2B	Decrement register pair HL by 1.
DEC A	3D	Decrement the accumulator by 1.
DEC B	05	Decrement register B by 1.
JP *nn*	C3 *n n*	Jump to address *nn*.
JP Z *nn*	CA *n n*	Jump on zero to address *nn*.
JP NZ *nn*	C2 *n n*	Jump on non-zero to address *nn*.
HALT	76	Halt.

Note: *n* is an 8 bit data item; *n n* is a 16 bit data item or address

Q1 *Write down the decimal equivalent of the following binary numbers, showing all your working.*

(*a*) *101 101*
(*b*) *111·11* *(5 min)*

A1 Binary numbers can be converted to their decimal equivalent by writing down the 'weight' of each bit and then adding them together.

(*a*) 1 0 1 1 0 1

$(1 \times 32) + (1 \times 8) + (1 \times 4) + (1 \times 1) = 45.$

$\therefore \quad 101\,101_2 = \underline{45_{10}}.$

(*b*) 1 1 1 · 1 1

$(1 \times 4) + (1 \times 2) + (1 \times 1) + (1 \times 0{\cdot}5) + (1 \times 0{\cdot}25) = 7{\cdot}75.$

$\therefore \quad 111{\cdot}11_2 = \underline{7{\cdot}75_{10}}.$

Q2 *Convert the two octal numbers given below into binary form, add them together, and give the answer in hexadecimal form.*

(*a*) *762*
(*b*) *470* *(4 min)*

A2 The numbers are first converted to binary form by writing down the 3 bit binary equivalent of each of the octal number.

(*a*) 7 6 2
111 110 010

(*b*) 4 7 0
100 111 000

They can then be added together.

	111 110 010
	100 111 000
Carry	1 1 1 1
	1 100 101 010

The answer is converted to hexadecimal form by grouping the bits in fours starting with the least-significant bit, and expressing each group as a hexadecimal number.

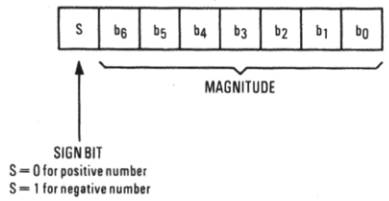
11 0010 1010

3 2 A

The result is $\underline{32A_{16}}$.

Q3 *Explain what is meant by 'two's complement notation'.* *(2 min)*

A3 *Two's complement notation* is a method used to represent numbers in digital systems. The most significant bit of each number is used to represent the sign of the number. For example, in an 8 bit system, bits 0 to 6 of the number represent its magnitude and bit 7 gives its sign, as shown below.



Q4 *State the rule for finding the two's complement of a number. Illustrate your answer by finding the two's complement of each number below.*

(*a*) *01 100 000*
(*b*) *11 000 100* *(5 min)*

A4 To find the two's complement of a number, invert the complete number, including the sign bit, and add one.

(*a*)

	01 100 000	$(+96_{10})$
Invert	10 011 111	
Add 1	1	
	10 100 000	(-96_{10})

(*b*)

	11 000 100	(-60_{10})
Invert	00 111 011	
Add 1	1	
	00 111 100	$(+60_{10})$

Q5 *Perform the following calculation using a two's-complement method:*

1 100 100 − 1 001 001.

(3 min)

A5 First find the two's complement of 1 001 001 by inverting and adding 1:

	1 001 001
Invert	0 110 110
Add 1	1
	0 110 111

Add the two's complement to 1 100 100:

	1 100 100
	0 110 111
Carry	11 1
	10 011 011

The result is 0011011; the overflow bit indicates that the result is positive.

Q6 *What is a register? Give three typical uses of the registers in a microprocessor.* *(4 min)*

A6 A register is an electronic circuit capable of storing a binary number; generally, it consists of a number of bistable circuits.

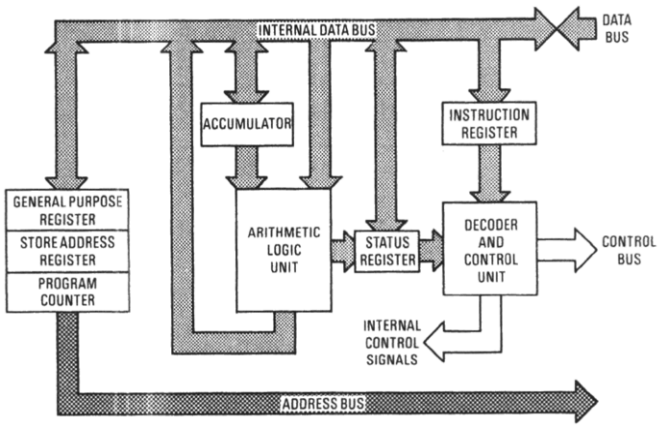
In a microprocessor, registers are used:

(*a*) to store data used in calculations etc,
(*b*) to store memory addresses, and
(*c*) to store the microprocessor instructions.

Q7 *Draw a diagram showing the internal structure of a typical microprocessor, showing in particular:*

(*a*) *the instruction register,*
(*b*) *the program counter,*
(*c*) *the store address register(s),*
(*d*) *the accumulator,*
(*e*) *the arithmetic logic unit,*
(*f*) *the status register (flags), and*
(*g*) *the control and timing devices.* *(8 min)*

A7 The sketch shows a typical 8 bit microprocessor based on the Z80.



Q8 *Select the correct answer to complete the following sentence:*

'The instruction register is ...'

(*a*) *the place where the address for the next instruction is stored.*
(*b*) *the place where the control signals come from.*
(*c*) *the place where an op-code is put during an instruction* FETCH *operation.*
(*d*) *the place where the results of logical instructions are put.* *(1 min)*

A8 (*c*) the place where an op-code is put during an instruction FETCH operation.

Q9 *Select the correct answer to complete the following sentence:*

'The program counter is ...'

(*a*) *a device for counting the number of lines in a program.*
(*b*) *the register which contains the address of the next instruction.*
(*c*) *a memory pointer used to move data in memory.*
(*d*) *a general-purpose register used as a counter.* *(1 min)*

A9 (*b*) the register which contains the address of the next instruction.

Q10 *Indicate which part of the instructions below is the operator and which is the operand.*

(*a*) *LD A, 80* *Hexadecimal code 3E 80*
(*b*) *JP 1234* *Hexadecimal code C3 34 12* *(3 min)*

A10

(*a*) LD A,		3E	is the operator
	80	80	is the operand
(*b*) JP		C3	is the operator
	1234	34	is the operand
		12	

[*Tutorial note:* The operator in each instruction specifies the function to be carried out. The operand specifies either data or an address to be used.]

Q11 *Explain how a microprocessor uses its program counter, address, data and control buses, instruction register, accumulator and arithmetic logic unit (ALU), when it encounters the instruction ADD A, 30 hex (hexadecimal code C6 30) in a program.* *(8 min)*

A11 The following sequence of events takes place:

(*a*) The contents of the program counter are placed on the address bus, and a memory read takes place.
(*b*) The program counter is incremented.
(*c*) The op-code C6 is read from memory and transferred over the data bus to the instruction register.
(*d*) The instruction is decoded.
(*e*) The contents of the program counter are placed on the address bus, and another memory read takes place.
(*f*) The program counter is incremented.
(*g*) The data value 30 hex is read from memory and is transferred over the data bus to one of the inputs of the ALU.
(*h*) The contents of the accumulator are added to the number 30 hex and the result is returned to the accumulator.

The final step (*h*) may be delayed until after the start of the next instruction FETCH. This is known as the *FETCH/EXECUTE overlap.*

Q12 *What is a machine-code monitor.* *(3 min)*

A12 A machine-code monitor is a microcomputer program, normally resident in read-only memory, which is executed automatically as soon as a microcomputer is switched on. It provides the machine with the basic operating functions such as keyboard scanning for data, display management, etc. It may also provide the user with the means to enter, modify and execute programs written in machine code.

Q13 *Explain why flow charts are important in the production of computer programs.* *(4 min)*

A13 Drawing a flow chart is generally one of the first steps in the production of a computer program. It is very important for a programmer to be able to plan his program logically, and the production of a flow chart is a convenient pictorial means of achieving this. With large programs, a flow chart is particularly important since different parts of the program may be interconnected in complex ways.

Once a flow chart has been produced, it is easy for other people to understand the program operation. In addition, the flow chart can be translated into whatever computer language is appropriate.

Q14 *The major groups of instructions in any microprocessor instruction set are:*

(*i*) *data movement,*
(*ii*) *data manipulation (arithmetic and logic), and*
(*iii*) *flow of control (test and branch).*

State, for each of the instructions below, which major group they belong to:

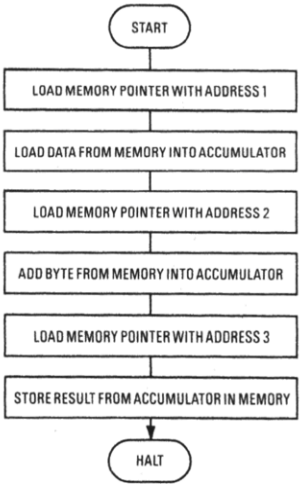
(*a*) *DEC HL;*
(*b*) *HALT;*
(*c*) *ADD A, (HL);*
(*d*) *LD HL, nn; and*
(*e*) *JP Z nn.* *(3 min)*

A14

Instruction	Group of Instructions
(*a*) DEC HL	(*ii*) Data Manipulation
(*b*) HALT	(*iii*) Flow of Control
(*c*) ADD A, (HL)	(*ii*) Data Manipulation
(*d*) LD HL, *nn*	(*i*) Data Movement
(*e*) JP Z *nn*	(*iii*) Flow of Control

Q15 Draw the flow chart, and produce the machine-code program under the headings Address, Hexadecimal Code, and Mnemonic, that will add together the data found in memory addresses 1508 hex and 37C3 hex, and place the result in memory address 511F hex. Start your program at address 1000 hex. *(10 min)*

A15



Address	Hexadecimal Code	Mnemonic
1000	21 08 15	LD HL, 1508 hex
1003	7E	LD A, (HL)
1004	21 C3 37	LD HL, 37C3 hex
1007	86	ADD A, (HL)
1008	21 1F 51	LD HL, 511F hex
100B	77	LD (HL), A
100C	76	HALT

[*Tutorial note:* This program could be written in other ways by using the complete Z80 instruction set, but the answer given is restricted to those given in the shortened instruction set given at the beginning of this paper.]

Q16 Draw a trace table to show the contents of all the relevant registers and memory addresses during the execution of the following program.

Address	*Hexadecimal Code*	*Mnemonic*
1000	*21 OC 10*	*LD HL, 100C hex*
1003	*06 7F*	*LD B, 7F hex*
1005	*7E*	*LD A, (HL)*
1006	*A0*	*AND B*
1007	*D6 13*	*SUB 13 hex*
1009	*23*	*INC HL*
100A	*77*	*LD (HL), A*
100B	*76*	*HALT*
100C	*B7*	*Data*
100D	*00*	*Data*

(5 min)

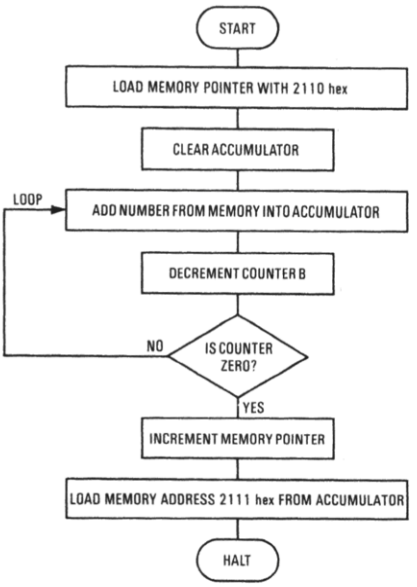
A16

Program Counter	Accumulator	Register B	Register Pair HL	Address 100D
1000	*X*	*X*	*XX*	00
1003	*X*	*X*	100C	00
1005	*X*	7F	100C	00
1006	B7	7F	100C	00
1007	37	7F	100C	00
1009	24	7F	100C	00
100A	24	7F	100D	00
100B	24	7F	100D	24

X = not defined

Q17 Multiplication can be performed by repeated addition. Draw a flow chart, and produce the machine-code program under the headings Address, Hexadecimal Code and Mnemonic, that will multiply the number in memory address 2110 hex by the number held in register B and place the result in memory address 2111 hex. Assume both of the initial numbers are between 1 and 16. Start the program at address 1000 hex. *(10 min)*

A17 Assuming register B and address 2110 hex are already loaded, then the flow chart is as shown in the sketch.

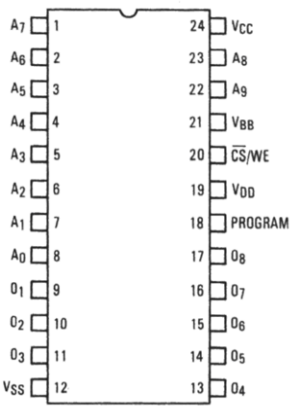


The program is given in the following table.

Address	Hexadecimal Code	Mnemonic
1000	21 10 21	LD HL, 2110 hex
1003	3E 00	LD A, 00
1005	86	ADD A, (HL)
1006	05	DEC B
1007	C2 05 10	JP NZ 1005 hex
100A	23	INC HL
100B	77	LD (HL), A
100C	76	HALT

Q18 With reference to Fig. 1, answer the following questions:

(*a*) *What type of memory chip is shown?*
(*b*) *How many memory locations does it have?*
(*c*) *How many bits are stored?* *(4 min)*



PIN NAMES

A_0–A_9	ADDRESS INPUTS
O_1–O_8	DATA OUTPUTS
$\overline{CS}$/WE	CHIP SELECT/WRITE ENABLE INPUT

Fig. 1

A18 (*a*) The memory chip is an electrically-programmable read-only memory (EPROM), as indicated by the PROGRAM pin.

(*b*) The chip has 10 address lines, and this indicates that there are 2^{10} locations; that is, 1024 locations.

(*c*) There are 8 data lines. The capacity of the chip is, therefore,

$$8 \times 1024 = 8192 \text{ bits.}$$

Q19 Name two types of buffer commonly found in microprocessor systems, and explain why each one is necessary. (*5 min*)

A19 The two types of buffer are

(*a*) unidirectional buffers, and
(*b*) bidirectional buffers.

A unidirectional buffer would be used on the address bus to increase the fan-out of the address-bus pins of the microprocessor. In a large system, often many memory devices and decoders are connected to the address bus. The severe loading problems this causes can be overcome by using a buffer to increase the drive current available on each address line.

A bidirectional buffer with tri-state outputs would be used on the data bus. Data can pass in both directions on the data bus, and so a bidirectional buffer is required. The buffer must also have the ability to go into a high-impedance (tri-state) condition, since other devices may need to use the common bus and must be able to do so without interference.

Questions and answers contributed by D. Turner

BTEC: DIGITAL TECHNIQUES A III

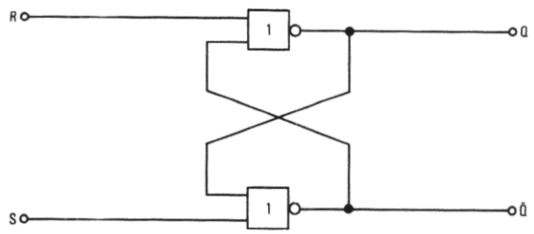
The following questions are based on the BTEC's standard unit U81/751. Students are advised to read the notes on p. 33

Q1 (*a*) *Draw a logic diagram to show how an SR latch could be constructed from*

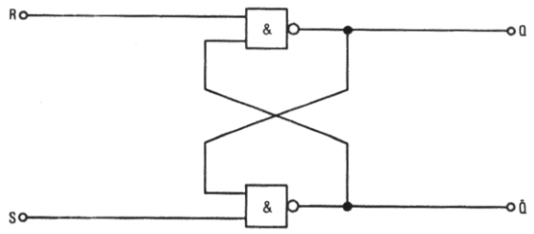
(*i*) *two* NOR *gates, and*
(*ii*) *two* NAND *gates.*

(*b*) *Write down the truth table for each circuit and comment on the significance of each input combination.* (*5 min*)

A1 (*a*) (*i*) NOR gates



(*ii*) NAND gates



(*b*) The two truth tables are shown below.

NOR gates

R	S	Q	$\bar{Q}$	Comment
0	0	Previous State		Memory
0	1	1	0	Set
1	0	0	1	Reset
1	1	0	0	Indeterminate

NAND gates

R	S	Q	$\bar{Q}$	Comment
0	0	1	1	Indeterminate
0	1	1	0	Set
1	0	0	1	Reset
1	1	Previous State		Memory

Q2 Draw the output waveform at Q if the input waveforms at R and S of an SR bistable circuit are as shown in Fig. 1. Assume that Q is initially at logic 0. (*2 min*)

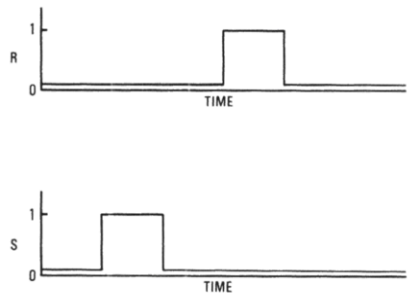
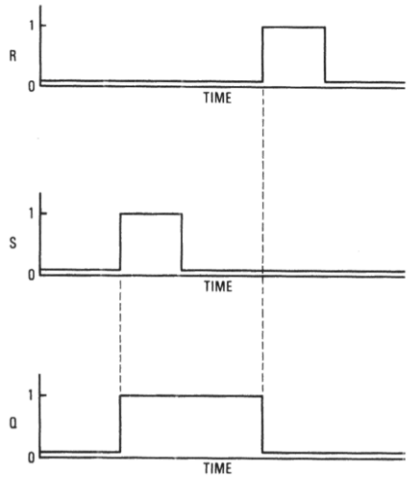


Fig. 1

A2 The circuit waveforms would be as shown in the sketch.



Q3 *Identify the circuit symbols shown in Fig. 2 and write down the truth table for each one.* (*5 min*)

(*a*) (*b*)

Fig. 2

A3 (*a*) The circuit symbol shown is a clocked SR bistable circuit and its truth table is given below.

Clock	S	R	Q	Q̄
0	0	1	Previous Q	Previous Q̄
1	0	1	0	1
0	0	0	0	1
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	1	1	1	0
1	1	1	Indeterminate	

(*b*) The circuit symbol shows a D-type bistable circuit, and its truth table is given below.

Clock	D	Q	Q̄
0	0	Previous Q	Previous Q̄
1	0	0	1
0	1	0	1
1	1	1	0

Q4 *In the circuit shown in Fig. 3, the input is held at a logic 1 and the outputs X and Y are 0 and 1 respectively. Explain the action of the circuit when one positive-going clock pulse is applied.* (*5 min*)

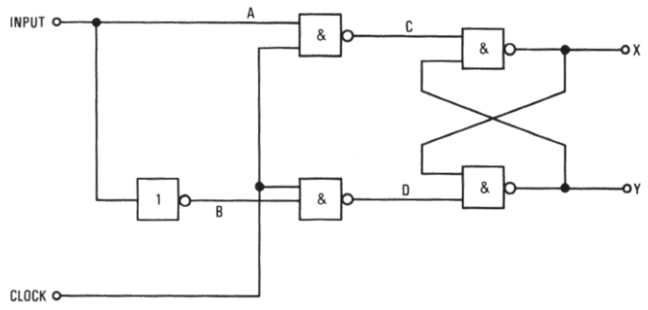


Fig. 3

A4 If point A in the circuit is at logic 1, then point B is at logic 0. This causes point D to be at logic 1 and, if the clock input is initially at logic 0, then point C is also at logic 1.

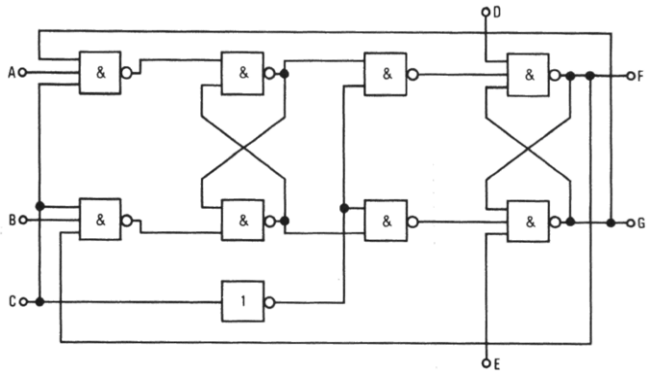
When the clock pulse goes to logic 1, point C falls to logic 0, causing point X to become logic 1. This signal is fed back and gated with the logic 1 from point D to force point Y to logic 0. When the clock pulse returns to logic 0, both points C and D become logic 1 and outputs X and Y remain unchanged.

The net result of the clock pulse is to change the state of both X and Y outputs.

Q5 *What advantages does a JK flip-flop circuit have over a clocked SR flip-flop circuit.* (*2 min*)

A5 A JK flip-flop circuit has one major advantage over an SR flip-flop circuit because it does not have an indeterminate state. If both inputs of an SR flip-flop circuit are connected to logic 1, then its outputs Q and Q̄ both assume the same state when the clock pulse is applied. However, if both inputs of a JK flip-flop circuit are connected to logic 1, the outputs toggle (change state) on each clock pulse.

Q6 *Identify the circuit shown in Fig. 4 and draw one symbol to represent the complete circuit, showing the correct designation for each terminal.* (*3 min*)



A6 The circuit is a JK master–slave flip-flop circuit with synchronous SET and RESET inputs. Its usual circuit symbol is shown in the sketch.

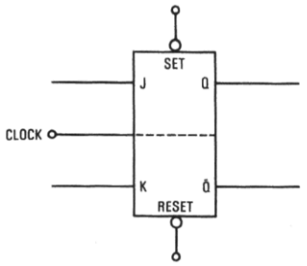


Fig. 4

Q7 *Complete the following sentence using one of the answers given below:*

'A JK bistable circuit can be used as a divide-by-two counting device by . . .

(*a*) *connecting the Q̄ output to the K input.*
(*b*) *connecting both J and K inputs to logic 1.*
(*c*) *connecting input J to Q and input K to Q̄.*
(*d*) *connecting input J to logic 1 and input K to logic 0.* (*2 min*)

A7 (*b*) connecting both J and K inputs to a logic 1.

Q8 *Explain the terms*

(*a*) *asynchronous,*
(*b*) *synchronous, and*
(*c*) *ripple-through delay*

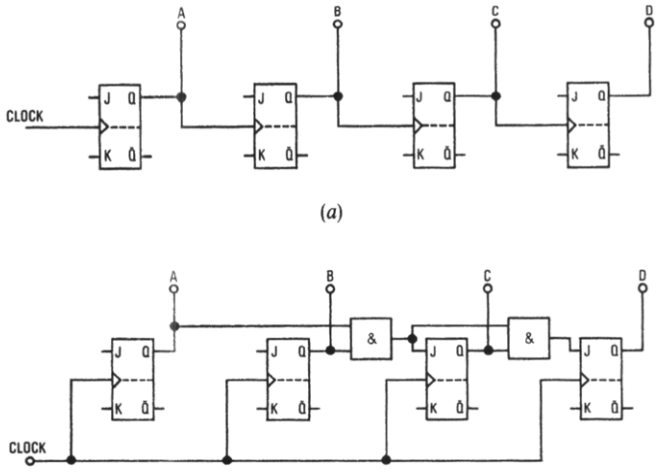
when applied to counter circuits. (*6 min*)

A8 (*a*) *Asynchronous* is a description given to a counter whose outputs do not all change at exactly the same moment. Generally, in an asynchronous counter, the clock pulse for any stage is derived from the output of the previous stage.

(*b*) *Synchronous* is the description given to a counter whose outputs all change at the same moment. Generally, all the stages of a synchronous counter are connected to the same clock line.

(*c*) *Ripple-through delay* is the delay present in an asynchronous counter between the change in output of the first bistable circuit and that of the last. If the propagation delay of an individual bistable circuit is t seconds, then the ripple through delay for an N-stage counter is Nt seconds.

Q9 *Identify the circuits shown in Fig. 5, and state which one is capable of operating at the highest clock rate.* (*2 min*)



(*a*)

(*b*)

Fig. 5

A9 Circuit (*a*) is an asynchronous divide-by-16 counter, and circuit (*b*) is a synchronous divide-by-16 counter.

The synchronous divide-by-16 counter is capable of operating at a higher clock rate while still giving meaningful outputs, since it does not suffer from ripple-through delay.

Q10 *List the count sequence in binary for the counter shown in Fig. 6. Output A is the least significant bit.* (*4 min*)

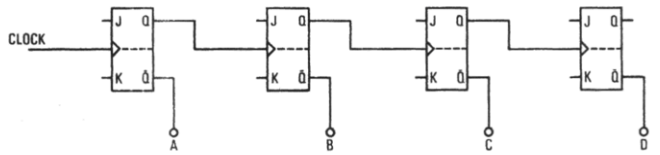


Fig. 6

A10 The counter shown is a binary down-counter, which has the following count sequence.

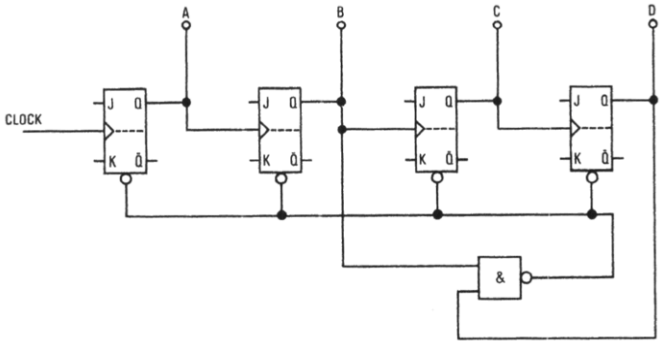
Clock	D	C	B	A
0	0	0	0	0
1	1	1	1	1
2	1	1	1	0
3	1	1	0	1
4	1	1	0	0
5	1	0	1	1
6	1	0	1	0
7	1	0	0	1
8	1	0	0	0
9	0	1	1	1
10	0	1	1	0
11	0	1	0	1
12	0	1	0	0
13	0	0	1	1
14	0	0	1	0
15	0	0	0	1
16	0	0	0	0

Q11 *Briefly explain why a decade counter is often required.* (*3 min*)

A11 A decade counter has 10 states, which can be used to represent 10 different numbers. Therefore, it has many applications, especially where there is a need for numbers to be displayed in decimal form. Such applications include cash registers, digital voltmeters and digital watches etc. Often, it is more convenient to use decade counters in a system and produce a decimal display directly from them, than to use binary counters and then to convert from binary to decimal before a display is produced.

Q12 *Draw a logic diagram to show how a decade counter can be produced from an asynchronous binary up-counter by adding one extra gate. What special feature must be present in the bistable circuits used?* (*5 min*)

A12 A decade counter can be produced from a binary counter by using the circuit shown in the sketch.



Each bistable circuit must have an asynchronous CLEAR or RESET input to allow its output to be reset to logic 0 immediately, irrespective of the state of the clock input.

Q13 *Which type of counter, either transistor-transistor-logic (TTL) or complementary metal-oxide-semiconductor (CMOS), would be preferred in the following applications. Give your reasons in each case.*

(*a*) *The first stage in a 20 MHz counter in equipment with a 5 V power supply derived from the mains*

(*b*) *A circuit which must divide a clock rate by 4096 and use the least number of chips possible.*

(*c*) *A battery-powered digital measuring system.*

(*5 min*)

A13 (*a*) A TTL counter would be used, since a CMOS device operates only at up to 2 MHz with a 5 V supply.

(*b*) A CMOS device would be used for this application. It would require 3 TTL chips to produce the required division ratio, whereas it could be achieved with one CMOS device (4040).

(*c*) A CMOS device has a much lower power dissipation than its TTL equivalent and would therefore be preferred for any battery-operated equipment.

Q14 *CMOS counters with more than 20 stages are currently available. What are the main limitations of such devices?* (*3 min*)

A14 There are two main limitations. Firstly, the maximum clock rate for such devices is only 2 MHz with a 5 V supply. This means that higher clock rates must be divided first by using TTL counters before the CMOS types can be used. Secondly, it is possible to connect only a selection of the counter stages to the pins of the chip. This restricts the number of division ratios available.

Q15 (*a*) *Clearly label the terminals of the diagram shown in Fig. 7.*

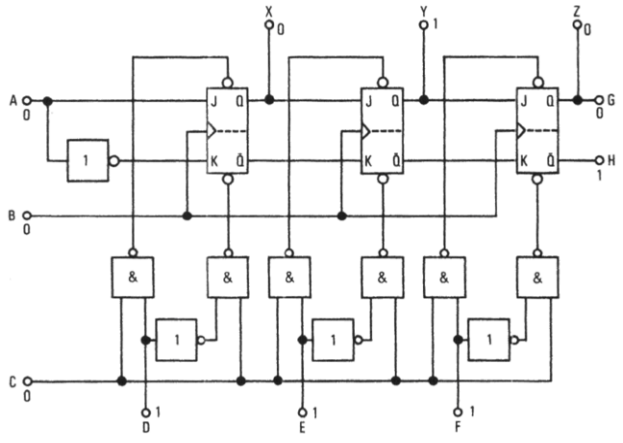
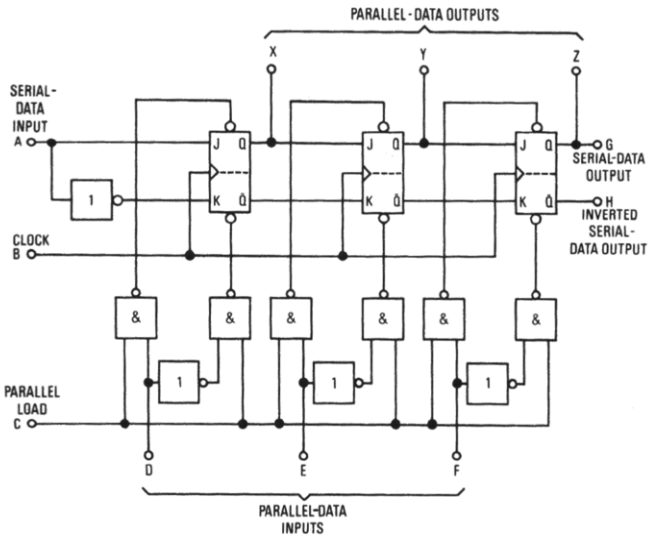


Fig. 7

(*b*) *Describe what happens to the contents of the register when one pulse is applied to point C, followed by three pulses to point B. Assume that the logic levels shown are present initially.* (*6 min*)

A15 (*a*)



(*b*) When one pulse is applied to input C, the parallel-load input, the parallel-data inputs are transferred into the register. After the pulse, points X, Y and Z will therefore all be at logic 1. If three pulses are then applied to the clock input B, the data shifts one place to the right for each pulse and the incoming data enters from the serial-data input A. The count in the register will be.

Clock Pulse No.	X	Y	Z
0	1	1	1
1	0	1	1
2	0	0	1
3	0	0	0

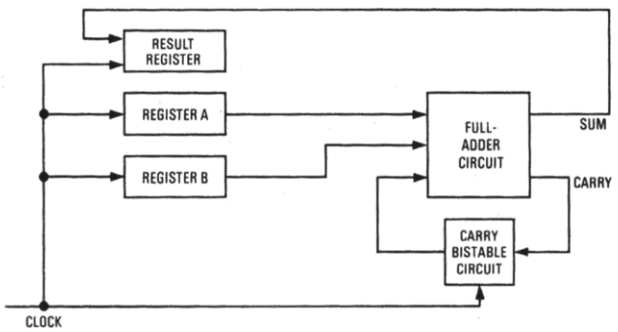
Q16 A 74194 device is described as being a 'universal shift register'. Explain what is meant by this. (*2 min*)

A16 A universal shift register exhibits the following features:

(*a*) it can be cleared,
(*b*) it can be used for serial or parallel input,
(*c*) it can be used for serial or parallel output, and
(*d*) it can shift data either to the right or to the left.

Q17 Draw a block diagram to show how a shift register can be used as part of a serial arithmetic circuit designed to add binary numbers. (*4 min*)

A17 The sketch shows a serial adder which uses three shift registers to store the two numbers to be added and the result.



Q18 Identify the circuit given in Fig. 8 and explain its operation. (*6 min*)

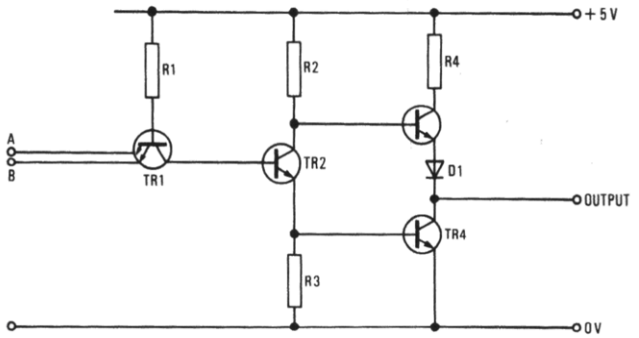


Fig. 8

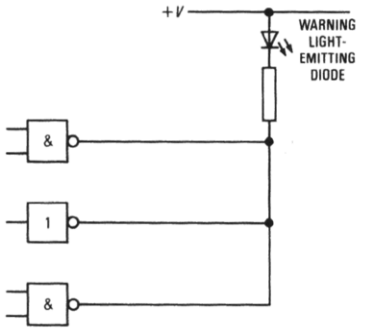
A18 The circuit is a 2-input NAND gate.

When either or both of the inputs A and B are held at a logic 0, current flows out of the emitter of transistor TR1 from its base. The base-collector junction of transistor TR1 behaves like a diode, that is, reverse biased, and therefore no current flows into the base of transistor TR2, causing transistor TR2 to be cut OFF. With no current flowing in transistor TR2, its emitter remains at 0 V and this keeps transistor TR4 cut OFF. Resistor R2 pulls the base of transistor TR3 towards +5 V, and base current flows into transistor TR3 turning it ON. The output voltage therefore rises to a logic 1 level.

If both inputs A and B are held at logic 1 level, the base-emitter junction of transistor TR1 is reverse biased. Current therefore flows through resistor R1 and the base-collector junction of transistor TR1 into the base of transistor TR2. Transistor TR2 turns ON and saturates. The voltage across resistor R3 rises to about 0·7 V and transistor TR4 turns ON, thus bringing the output voltage to logic 0 level. The collector voltage of transistor TR2 is only about 0·9 V, which is insufficient to turn ON transistor TR3 since it has diode D1 in series with its base-emitter junction. Thus, transistor TR3 remains OFF, and transistor TR4 ON, producing logic 0 level at the output.

Q19 Give an example of the application of an open-collector gate. (*4 min*)

A19 Open-collector logic gates have no pull-up resistor inside the gate, and this means that an external pull-up resistor must be supplied. However, open-collector logic gates also offer the possibility of connecting a number of gates to the same pull-up circuit, as shown in the sketch.



The circuit shows how a warning light can be operated by any of the gates connected to it. Each gate has an open-collector output.

Q20 Choose one of the answers below to complete the following sentence:

'Emitter-coupled-logic (ECL) gates are often preferred to transistor-transistor-logic gates because . . .'

(*a*) *they dissipate very little power even at very high speed.*
(*b*) *their transistors saturate, giving much more accurate logic signals.*
(*c*) *many more ECL circuits are available in integrated circuit form.*
(*d*) *their transistors do not saturate, and this makes high-speed operation possible.* (*1 min*)

A20 (*d*) their transistors do not saturate, and this makes high-speed operation possible.

Questions and answers contributed by D. Turner

SCOTTISH TECHNICAL EDUCATION COUNCIL

Higher Certificate and Certificate Courses in Electrical and Electronic Engineering

The questions given below are from examination papers set by the Scottish Technical Education Council (SCOTEC) and are reproduced with the permission of the SCOTEC. The answers given have been prepared by independent authors. Sometimes, additional tutorial information is given; this is enclosed within square brackets to distinguish it from the information that would be expected of students under examination conditions. Answers to some questions are occasionally omitted because of insufficient space.

SCOTEC: ELECTRICAL PRINCIPLES III (Component B) 1983

Students were expected to answer any four questions. The time allowed for the paper was 1½ hours

The following table describes some of the instructions given in the instruction set used for this subject. In the table, y refers to a 4-digit hexadecimal memory address, and x refers to a 2-digit hexadecimal item of data.

AND y	This instruction performs a logical AND between the contents of memory location y and the accumulator. The result is stored in the accumulator. If the result is zero, the zero flag is set to logic 1.
BRK	This instruction stops the program.
BNZ y	Branch to memory location y if the zero flag is set to logic 0.
BZE y	Branch to memory location y if the zero flag is set to logic 1.
LDA #x	This instruction loads the accumulator with the data held in the next location; that is, x.
LDA y	This instruction loads the accumulator with the data held in memory location y.
STA y	The contents of the accumulator are stored in memory location y.
SUB y	This instruction subtracts the contents of memory location y from the accumulator. The result is stored in the accumulator. If the result is zero, the zero flag is set to logic 1.

Q1 *The circuit shown in Fig. 1 is connected to a 10 mV 15 kHz supply. Evaluate:*

(a) the circuit impedance,
(b) the current, and
(c) the voltages across terminals AB and BC.

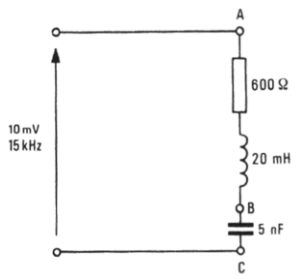


Fig. 1

A1 (*a*) The inductive reactance, X_L, is given by $2\pi fL$, where f is the frequency and L is the inductance.

$$\therefore \quad X_L = 2\pi \times 15 \times 10^3 \times 20 \times 10^{-3} = 1885\ \Omega.$$

The capacitative reactance, X_C, is given $1/(2\pi fC)$, where C is the capacitance.

$$\therefore \quad X_C = \frac{1}{2\pi \times 15 \times 10^3 \times 5 \times 10^{-9}} = 2122\ \Omega.$$

If R is the resistance, then the total impedance of the circuit, Z, is given by

$$\therefore \quad Z = \sqrt{\{R^2 + (X_L - X_C)^2\}} = \sqrt{\{600^2 + (1885 - 2122)^2\}},$$
$$= \underline{645\ \Omega.}$$

(*b*) The current, I, is given by V/Z, where V is the input voltage.

$$\therefore \quad I = \frac{10 \times 10^{-3}}{645} = \underline{15{\cdot}5\ \mu A.}$$

(*c*) The voltage across terminals AB, V_{AB}, is given by IZ_{LR}, where Z_{LR} is the total impedance of the resistor and the inductor

$$\therefore \quad V_{AB} = 15{\cdot}5 \times 10^{-6} \times \sqrt{(600^2 + 1885^2)} = \underline{30{\cdot}6\ \text{mV.}}$$

The voltage across terminals BC, V_{BC}, is given by

$$V_{BC} = IX_C = 15{\cdot}5 \times 10^{-6} \times 2122 = \underline{32{\cdot}9\ \text{mV.}}$$

Q2 *For the amplifier shown in Fig. 2, determine the current gain and the voltage gain.*

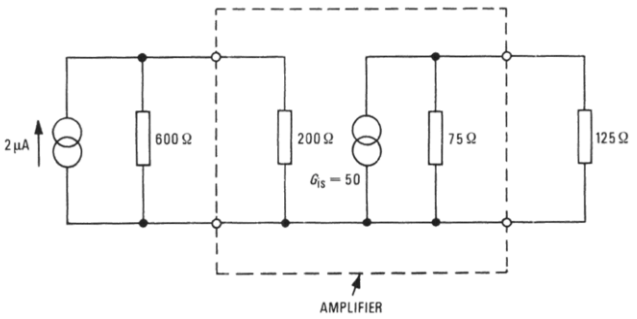


Fig. 2

A2 The input current to the amplifier is given by

$$I_i = \frac{600}{600 + 200} \times 2 \times 10^{-6} = 1{\cdot}5 \times 10^{-6}\ \text{A.}$$

The output current to the load is given by

$$I_0 = 1{\cdot}5 \times 10^{-6} \times 50 \times \frac{75}{75 + 125} = 28{\cdot}1 \times 10^{-6}\ \text{A.}$$

The current gain, G_i, is given by

$$G_i = \frac{I_0}{I_i} = \frac{28{\cdot}1}{1{\cdot}5} = \underline{18{\cdot}8.}$$

The voltage gain, G_V, is given by

$$G_V = \frac{\text{output voltage}}{\text{input voltage}} = \frac{I_0 \times 125}{I_i \times 200},$$
$$= \frac{28{\cdot}1 \times 10^{-6} \times 125}{1{\cdot}5 \times 10^{-6} \times 200},$$
$$= \underline{11{\cdot}7.}$$

Q3 *In a microprocessor system, a single-byte number is located at 0060 and a single-byte number is available at the input A001. The program of this system is given below.*

Explain each instruction of the following program.

```
LDA 0060
STA 0040
LDA A001
SUB 0040
STA 0041
BRK
```

Describe the purpose of this program.

A3 The instructions are explained in the following table:

Instruction	Explanation
LDA 0060	Load accumulator with number stored in location 0060
STA 0040	Store number held in the accumulator in location 0040
LDA A001	Load accumulator with number at input port A001
SUB 0040	Subtract number stored in location 0040 from that in the accumulator
STA 0041	Store the result of the previous operation, held in the accumulator, in location 0041
BRK	End program

The program determines the difference between the number input at port A001 and the number stored in location 0060, and subsequently stores the result.

Q4 *A 100 mH inductor of resistance 600 Ω is connected across a 10 V DC supply.*
Determine:

(*a*) *the initial current,*
(*b*) *the final current, and*
(*c*) *the time taken for the current to rise to 10 mA.*

A4 (*a*) The initial current is 0 A.
(*b*) The final current, I_∞, is V/R, where V is the supply voltage and R is the resistance.

$$\therefore \quad I_\infty = \frac{10}{600} = \underline{16{\cdot}7 \text{ mA.}}$$

(*c*) The current, i, after t seconds is given by

$$i = I_\infty(1 - e^{-Rt/L}),$$

where L is the inductance. The time for the current to rise to 10 mA is calculated from

$$10 \times 10^{-3} = 16{\cdot}7 \times 10^{-3}(1 - e^{-Rt/L}).$$

$$\therefore \quad t = \frac{L}{R} \times 0{\cdot}91 = \frac{100 \times 10^{-3} \times 0{\cdot}91}{600},$$

$$= \underline{0{\cdot}12 \text{ ms.}}$$

Q5 *A hoist is fitted with a protective device which operates at a height of 2·0 m. Above 2·0 m, the protective device inputs logic 0 to the controlling microprocessor system.*
As the hoist descends toward the 2·0 m limit, the input changes to logic 1. Should the hoist descend past the 2·0 m limit, the input returns to logic 0.
Write a program that continually checks the state of the input signal at A001 and which outputs the byte 20 (which stops the hoist) at A000 after the protection device input has changed from 0 to 1 back to 0.

A5

```
    LDA #00
    STA 0040
→   LDA A001
    AND 0040
    BZE
→   LDA A001
    AND 0040
    BNZ
    LDA #20
    STA A000
    BRK
```

Q6 *A 500 V 30 kW DC series motor operates at 750 r/min on full load and develops a torque of 380 N m.*
Calculate the speed at which the motor will operate when the load is reduced until the output torque is 250 N m. It may be assumed that all losses can be neglected and that the magnetic circuit remains unsaturated.

A6

$$I_1 = \frac{P_1}{V} = \frac{30 \times 10^3}{500} = 60 \text{ A.}$$

$$\frac{M_1}{M_2} = \frac{I_1^2}{I_2^2}, \text{ since } M \propto \Phi I \propto I^2.$$

$$\therefore \quad I_2 = \sqrt{\left(\frac{250}{380} \times 60^2\right)} = 48{\cdot}7 \text{ A.}$$

But, $E \propto \Phi N \propto IN.$

Since there are no circuit losses, $E = V$.

$$\therefore \quad I_1 N_1 = I_2 N_2.$$

$$\therefore \quad N_2 = \frac{I_1 N_1}{I_2} = \frac{60 \times 750}{48{\cdot}7},$$

$$= \underline{925 \text{ r/min.}}$$

Key to symbols used in this solution:
I is the current supplied to the load, I_1 being the initial current, and I_2 the final current.
M is the torque, M_1 being the initial torque and M_2 the final torque.
P_1 is the initial power developed in the load.
V is the voltage across the load.
Φ is the flux.
E is the developed EMF.
N is the speed of the motor, N_1 being the initial speed, and N_2 the final speed.

Answers contributed by I. McKenzie Smith

As an experiment, model answers to a Higher Certificate examination paper set by SCOTEC—Telecommunication Transmission Systems V— are given below. The editors hope that this paper will be of use not only to SCOTEC students studying this subject, but also to TEC students studying at the Higher Certificate level. Comments on this, and suggestions on how the *Supplement* could be developed to include Higher Certificate material on a more regular basis, would to be most welcome from both students and those concerned with teaching or tutoring. Indeed, comments on any of the material included in the *Supplement* are invited. Letters should be addressed to the Deputy Managing Editor, *British Telecommunications Engineering*, LCS/P5.1.1, Room 704B, Lutyens House, 1–6 Finsbury Circus, London EC2M 7LY.

SCOTEC: TELECOMMUNICATION TRANSMISSION SYSTEMS V 1983

Students were expected to attempt five questions. The time for this paper was three hours

Q1 (*a*) *Define the following terms:*

(*i*) *propagation coefficient, and*
(*ii*) *phase-change coefficient.*

(*b*) *Show that the characteristic impedance of a symmetrical T network is*

$$Z_0 = (Z_{sc} Z_{oc})^{1/2}.$$

(*c*) *Determine the characteristic impedance of the network shown in Fig. 1.*

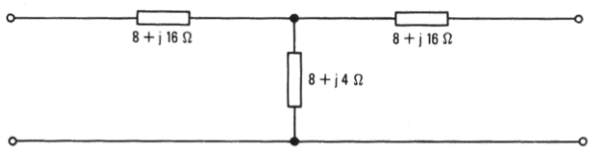
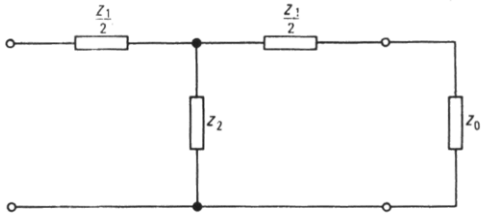


Fig. 1

A1 (*a*) (*i*) The propagation coefficient is defined as the natural logarithm of the phasor ratio of steady-state amplitudes of a wave at a specified frequency, at points in the direction of propagation separated by a unit length; the line is assumed to be uniform, and either infinite in length or terminated in its characteristic impedance.

(*ii*) The propagation coefficient can be written as $\gamma = \alpha + j\beta$; β is the phase-change coefficient and is the phase difference between the currents, or voltages, at the beginning and end of a unit length of line.

(*b*) The sketch shows a T network made up of impedances and terminated in its characteristic impedance, Z_0.



Z_0 = input impedance.

$$\therefore \quad Z_0 = \frac{Z_1}{2} + \frac{\left(\frac{Z_1}{2} + Z_0\right)Z_2}{\frac{Z_1}{2} + Z_0 + Z_2}.$$

$$\therefore \quad Z_0 = \sqrt{\left(Z_1Z_2 + \frac{Z_1^2}{4}\right)}. \qquad \ldots\ldots (1)$$

If the impedance Z_0 in the circuit shown in the sketch is short circuited, then the input impedance, Z_{sc}, is given by

$$Z_{sc} = \frac{Z_1}{2} + \frac{\frac{Z_1Z_2}{2}}{\frac{Z_1}{2} + Z_2},$$

$$= \frac{\frac{Z_1^2}{4} + Z_1Z_2}{\frac{Z_1}{2} + Z_2}. \qquad \ldots\ldots (2)$$

If the impedance Z_0 in the sketch is open circuited, then the input impedance, Z_{oc}, is given by

$$Z_{oc} = \frac{Z_1}{2} + Z_2, \qquad \ldots\ldots (3)$$

From equations (2) and (3),

$$Z_{sc}Z_{oc} = \left(\frac{\frac{Z_1^2}{4} + Z_1Z_2}{\frac{Z_1}{2} + Z_2}\right)\left(\frac{Z_1}{2} + Z_2\right),$$

$$= \frac{Z_1^2}{4} + Z_1Z_2.$$

Hence, $$\sqrt{(Z_{sc}Z_{oc})} = \sqrt{\left(\frac{Z_1^2}{4} + Z_1Z_2\right)}.$$

But, the right-hand side of this equation = Z_0 (from equation (1)).

Thus, $$\underline{Z_0 = \sqrt{(Z_{sc}Z_{oc})}.} \qquad \text{QED}$$

(*c*) $$Z_{oc} = (16 + j20)\ \Omega.$$

$$Z_{sc} = 8 + j16 + \frac{(8 + j16)(8 + j4)}{16 + j20},$$

$$= (12{\cdot}88 + j19{\cdot}90)\ \Omega.$$

But, $$Z_0 = \sqrt{(Z_{oc}Z_{sc})},$$

$$= \sqrt{(16 + j20)(12{\cdot}88 + j19{\cdot}90)},$$

$$= \underline{14{\cdot}4 + j19{\cdot}98\ \Omega} \text{ or } \underline{24{\cdot}64\ \angle 54{\cdot}2^\circ\ \Omega.}$$

Q2 (*a*) *A transmission line is terminated in a correctly matched load. The line constants per loop kilometre are*

$$R = 600\ \Omega,\ L = 60\ mH,\ C = 0{\cdot}05\ \mu F,\ \text{and}\ G = 0.$$

The input signal voltage is 5·0 V at a frequency of 10 kHz. Calculate the line voltages and their respective phase angles at 500 m intervals along the line, and hence plot a polar diagram of the voltage along the line for about one wavelength.

(*b*) *The voltage across the matched load is 360° out of phase with the sending-end voltage. From the polar diagram, determine the length of the transmission line and hence the current in the load.*

A2 (*a*) The propagation coefficient, γ, is given by

$$\gamma = \{(R + j\omega L)(G + j\omega C)\}^{1/2},$$

where $\omega = 2\pi \times$ frequency.

$$\gamma = \{(600 + j2\pi \times 10 \times 10^3 \times 60 \times 10^{-3}) \times (0 + j2\pi \times 10 \times 10^3 \times 50 \times 10^{-9})\}^{1/2},$$

$$= 3{\cdot}463\ \angle 85{\cdot}479^\circ \text{ or } 0{\cdot}273 + j3{\cdot}452.$$

If V_0 is the input voltage to the transmission line, then the voltage at a distance of l kilometres along the line is

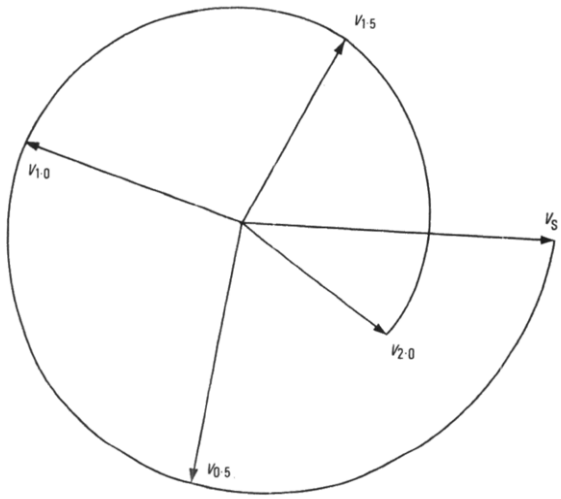
$$V_l = V_0 e^{-\gamma l}.$$

For $l = 500$ m,

$$\gamma l = 0{\cdot}137 + j1{\cdot}726.$$

$$\therefore \quad V_{0{\cdot}5} = V_0 \times 0{\cdot}872\ \angle -99^\circ.$$

The voltage phasors at 500 m intervals are each displaced by -99° and are in the ratio 0·872 : 1 (see sketch).



(*b*) For 360° phase shift, the length of line is

$$\frac{360}{99} \times 0{\cdot}5 = \underline{1{\cdot}82\ \text{km.}}$$

The characteristic impedance, Z_0, is given by

$$Z_0 = \sqrt{\left(\frac{R + j\omega L}{G + j\omega C}\right)},$$

$$= \sqrt{\left(\frac{600 + j2\pi \times 10 \times 10^3 \times 60 \times 10^{-3}}{0 + j2\pi \times 10 \times 10^3 \times 50 \times 10^{-9}}\right)},$$

$$= 1102\ \angle -4{\cdot}5^\circ\ \Omega.$$

From the diagram, $V_{1{\cdot}82} = 3{\cdot}0\ \angle -360^\circ$ V.

$$\therefore \quad \text{the current, } I = \frac{3{\cdot}0\ \angle -360^\circ}{1100\ \angle -4{\cdot}5^\circ}.$$

$$|I| = \underline{2{\cdot}7\ \text{mA.}}$$

[*Tutorial note*: The angle was not required in the question.]

Q3 (*a*) *Outline the main features of shunt compensation equalisers and indicate a type of distortion for which they would be appropriate.*

(*b*) *A symmetrical-T attenuator is shown in Fig. 2. The characteristic impedance of the network is* Z_0 *and the loss ratio is* A_L. *Show that*

$$R_1 = \frac{2(A_L - 1)}{A_L + 1} Z_0 \quad \text{and} \quad R_2 = \frac{2A_L}{A_L^2 - 1} Z_0.$$

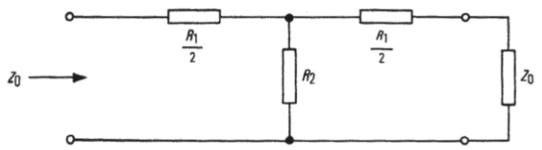


Fig. 2

A3 (*a*) The insertion loss of a shunt equaliser varies with frequency. The equaliser causes reflections because the line is no longer correctly terminated, and the reflection loss varies with frequency. They are used on audio-frequency speech circuits to compensate for frequency distortion.

(*b*) The loss ratio, A_L, is given by

$$A_L = 1 + \frac{R_1}{2R_2} + \frac{Z_0}{R_2}. \qquad \ldots\ldots (1)$$

But the input impedance, Z_0, of the network

$$= \frac{R_1}{2} + \frac{R_2\left(\frac{R_1}{2} + Z_0\right)}{R_2 + \frac{R_1}{2} + Z_0}.$$

$$= \frac{R_1}{2} + \frac{\frac{R_1}{2} + Z_0}{A_L}.$$

$$\therefore \quad R_1 = \frac{2(A_L - 1)}{A_L + 1} Z_0. \qquad \text{QED}$$

Substituting for R_1 in equation (1) gives:

$$A_L = 1 + \frac{Z_0(A_L - 1)}{R_2(A_L + 1)} + \frac{Z_0}{R_2}.$$

$$\therefore \quad A_L - 1 = \left(\frac{2A_L}{A_L + 1}\right)\frac{Z_0}{R_2}.$$

$$\therefore \quad R_2 = \frac{2A_L}{A_L^2 - 1} Z_0. \qquad \text{QED}$$

Q4 A 5 km transmission line has an attention coefficient of 0·9 dB/km and a phase-change coefficient of 144 °/km. The characteristic impedance is 600 Ω and is purely resistive.

The sending-end voltage is 2·0 V. The receiving end is connected to a matched generator of terminal voltage 1·0 V. The frequency of the generator is the same as that of the supply and the signals are in phase.

Find the current in the generator.

A4 The attenuation coefficient, $\alpha = 0{\cdot}9$ dB/km $= 0{\cdot}1037$ N/km.

The phase-change coefficient, $\beta = 144$ °/km $= 2{\cdot}513$ rad/km.

The voltage at the receiving end due to the generator

$$= 2{\cdot}0e^{-5(\alpha + j\beta)},$$

$$= 2{\cdot}0e^{-5 \times 0{\cdot}1037} \angle 5 \times 144°,$$

$$= 1{\cdot}19 \angle 720° \text{ V} \equiv 1{\cdot}19 \angle 0° \text{ V}.$$

$\therefore$ current in the generator

$$= \frac{1{\cdot}19 - 1{\cdot}0}{600} = \underline{0{\cdot}32 \text{ mA}}.$$

Q5 A loss-free transmission line has a characteristic impedance of 600 $\angle 0°$ *Ω and is terminated by a load of 6000* $\angle 0°$ *Ω. The sinusoidal sending-end voltage is 2·0 V RMS. Draw a graph showing the variation of the magnitude of the voltage along the line. (Only one wavelength of the line need be illustrated.)*

What is the least distance, in wavelengths, between points where the voltage is 2·0 V.

A5 The voltage reflection coefficient, ρ, is given by

$$\rho = \frac{Z_L - Z_0}{Z_L + Z_0},$$

where Z_L is the impedance of the load, and Z_0 is the characteristic impedance of the line.

$$\therefore \quad \rho = \frac{6000 - 600}{6000 + 600} = 0{\cdot}818 \angle 0°.$$

The maximum voltage, V_{max}, occurs at the termination and at points $\lambda/2$, λ etc. from the termination, and is given by

$$V_{max} = (1 + 0{\cdot}818)V_s,$$

where V_s is the incident voltage.

$$\therefore \quad V_{max} = 3{\cdot}64 \text{ V}.$$

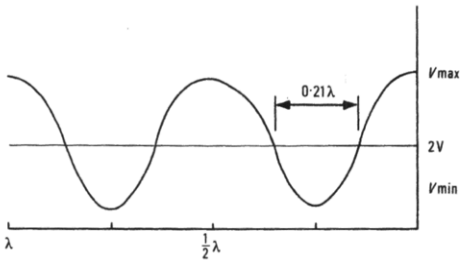
The minimum voltage, V_{min}, occurs at points $\lambda/4$, $3\lambda/4$ etc. from the termination, where V_{min} is given by

$$V_{min} = (1 - 0{\cdot}818)V_s = 0{\cdot}364 \text{ V}.$$

The voltage, V, at points $\lambda/8$, $3\lambda/8$ etc. from the termination is given by

$$V = \sqrt{(1^2 + 0{\cdot}818^2)}V_s = 2{\cdot}583 \text{ V}.$$

The graph is shown in the sketch.



The least distance between points where the voltage is 2·0 V is $\underline{0{\cdot}21\lambda}$.

Q6 (*a*) *Explain how standing waves result from reflections that occur with mismatched loads, and hence derive an expression for the voltage reflection coefficient.*

(*b*) *A 10·0 km long transmission line has the following constants per loop kilometre:*

$$R = 6{\cdot}5\ \Omega,\ L = 2{\cdot}3\ mH,\ C = 0{\cdot}005\ \mu F,\ \text{and}\ G = 3{\cdot}0\ \mu S.$$

The line is terminated with a resistive load of 600 Ω. The sending-end signals applied to the line are 10·0 V at 2664 Hz and 5·0 V at 1732 Hz.

Determine the amplitude of EACH *signal at the load.*

A6 (*a*) When a transmission line is terminated in its characteristic impedance, the voltage waves travelling down the line behave as they do in an infinitely long line until the point of mismatch is reached. Here the voltage waves are partly absorbed by the load impedance and are partly reflected back along the line. The summation of incident and reflected waves gives rise to a pattern of standing waves.

The voltage at the load is

$$V_L = V^+ + V^-, \qquad \ldots\ldots (1)$$

where V^+ is the voltage of the incident wave, and V^- the voltage of the reflected wave.

The current in the load, I_L, is given by

$$I_L = \frac{V^+}{Z_0} - \frac{V^-}{Z_0}, \qquad \ldots\ldots (2)$$

where Z_0 is the characteristic impedance.

Hence, adding equations (1) and (2) gives

$$2V^+ = V_L + I_L Z_0, \qquad \ldots\ldots (3)$$

and subtracting equation (2) from equation (1) gives

$$2V^- = V_L - I_L Z_0. \qquad \ldots\ldots (4)$$

Dividing equation (3) by equation (4) gives

$$\frac{V^+}{V^-} = \frac{V_L + I_L Z_0}{V_L - I_L Z_0} = \frac{Z_L + Z_0}{Z_L - Z_0}.$$

$$\therefore \quad V^- = \frac{Z_L - Z_0}{Z_L + Z_0} V^+.$$

But $V^- = \rho V^+$, where ρ is the reflection coefficient.

$$\therefore \quad \underline{\rho = \frac{Z_L - Z_0}{Z_L + Z_0}}.$$

(*b*) **2646 Hz signal**
The propagation coefficient, γ, is given by

$$\gamma = \{(R + j\omega L)(G + j\omega C)\}^{1/2},$$

where ω is $2\pi \times$ frequency.

$$\therefore \quad \gamma = \{(6{\cdot}5 + j2\pi \times 2664 \times 2{\cdot}3 \times 10^{-3}) \times (3 \times 10^{-6} + j2\pi \times 2664 \times 5 \times 10^{-9})\}^{1/2},$$
$$= \{(6{\cdot}5 + j38{\cdot}5)(3 \times 10^{-6} + j83{\cdot}7 \times 10^{-6})\}^{1/2},$$
$$= 0{\cdot}057 \angle 84{\cdot}2°.$$

Now, $$Z_0 = \left(\frac{R + j\omega L}{G + j\omega C}\right)^{1/2},$$

$$= \left(\frac{6{\cdot}5 + j38{\cdot}5}{3 \times 10^{-6} + j83{\cdot}7 \times 10^{-6}}\right)^{1/2} = 683 \angle -3{\cdot}8° \ \Omega.$$

The incident voltage at the termination, V^+, is given by

$$V^+ = V_s e^{-\gamma l},$$

where V_s is the voltage across the line at the sending end, and l is the distance of the load from the sending end along the line.

$$\therefore \quad |V^+| = 10e^{-0{\cdot}057 \times 10 \cos 84{\cdot}2} = 9{\cdot}44 \text{ V}.$$

The amplitude of the total voltage at the load is

$$|V_L| = |V^+| \times |(1 + \rho)|$$
$$= 9{\cdot}44 \times \left|\left(1 + \frac{600 - 683 \angle -3{\cdot}8}{600 + 683 \angle -3{\cdot}8}\right)\right|,$$
$$= 9{\cdot}44 \times |(1 + 0{\cdot}0727 \angle -27{\cdot}02°)|,$$
$$= \underline{10{\cdot}06 \text{ V}}.$$

1732 Hz signal

$$\gamma = \{(6{\cdot}5 + j2\pi \times 1732 \times 2{\cdot}3 \times 10^{-3}) \times (3 \times 10^{-6} + j2\pi \times 1732 \times 5 \times 10^{-9})\}^{1/2},$$
$$= 0{\cdot}0375 \angle 81{\cdot}1°.$$

$$Z_0 = \left(\frac{25{\cdot}86 \angle 75{\cdot}4°}{5{\cdot}44 \times 10^{-5} \angle 86{\cdot}8°}\right)^{1/2} = 689 \angle -5{\cdot}7° \ \Omega.$$

$$|V^+| = 5e^{-0{\cdot}0375 \times 10 \cos 81{\cdot}1} = 4{\cdot}72 \text{ V}.$$

$$|V_L| = 4{\cdot}72 \times \left|\left(1 + \frac{600 - 689 \angle -5{\cdot}7}{600 + 689 \angle -5{\cdot}7}\right)\right|,$$
$$= 4{\cdot}72 \times |(1 + 0{\cdot}085 \angle -35{\cdot}6°)|,$$
$$= \underline{5{\cdot}05 \text{ V}}.$$

Q7 *(a) Describe the construction and uses of monomode and multimode fibres.*
(b) State the operational properties of LEDs suitable for use as sources.
(c) Compare LED/multimode fibre systems with laser/monomode fibre systems.

Q8 *Outline, with the aid of suitable diagrams,* EACH *of the following types of distortion:*

(a) harmonic, and
(b) phase/amplitude.

Answers contributed by I. McKenzie Smith

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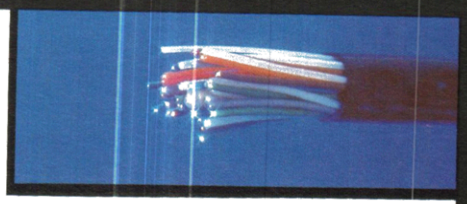

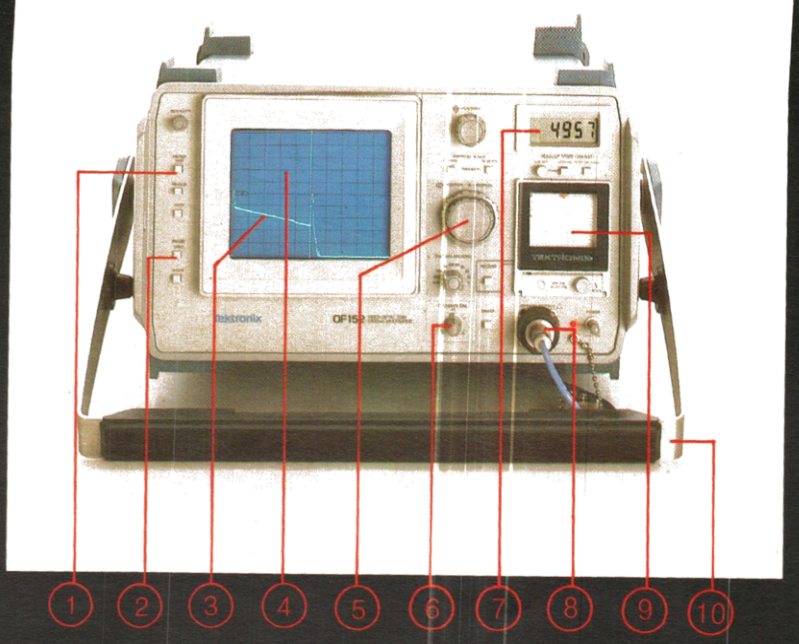

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